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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,943	02/26/2004	Mitrajit Chatterjee	IDT-1872	6684

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,943	CHATTERJEE ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 32-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-31* is/are rejected.

7)☒ Claim(s) *22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II (Claims 16-31), in the reply filed on December 12, 2006 is acknowledged.

Claims 1-15 and 32-37 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

This is a non-Final Office Action in response to RESTRICTION REQUIREMENT. Claims 16-31 are presently under examination. Claims 1-37 are pending.

Claim Objections

Claims 22-24 are objected to because of the following informalities:

Claim 22, the expression "so that" should be replaced with the term "wherein" to better define the synchronization function of the controller.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent,

except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-21 and 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Koschella (US-Patent No. 7,054,121), Application No. 10/117975, filed: April 8, 2002.

Regarding independent Claims 16, 25, Koschella discloses a processor-memory system with a protection circuit, Fig. 1, comprising:

A memory (memory device 3) including a protected area (B0, B1,Bi,. . Bn) or segments, that have to be treated differently in the event of an unauthorized external memory access, which is protected by a protection circuit 1.

A JTAG interface (externally accessible Data interface 6) known as Joint Test Action Group (JTAG), which is activated via a suitable external signal s1, which in the case of processors and microcontrollers is commonly referred to as "TEST" and "JTAG", respectively. Data d1 can be read or written into the memory device 3 through the externally accessible data interface 6.

Authorization logic (logic device 5.1, where the authorization logic device 5.1 is part of a controller (control circuit 5), which produces an area read enable signal $RE_{memory\ i}$ or an area write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area Bi, if the access authorization check in the logic device 5.1 using the signals RE, WE, OPC, $CE_{memory\ i}$ and the signals TEST and JTAG determines an authorized access. The basic access permission for the selected memory area Bi is

retrieved from the MPCR 7. In the event of an unauthorized access, the output of the signal $RE_{memory\ i}$ or $WE_{memory\ i}$, will be blocked by the logic device 5.1, as shown in Fig. 4, which is similar to that of Fig. 1.

Regarding Claim 17, 26, Koschella discloses memory device 3, which can be implemented as a Non-Volatile Random-Access-Memory (NVRAM), Fig. 1.

Regarding Claim 18, 27, Koschella discloses a processor CPU 2, Fig. 1, where the authorization logic device 5.1 combines the area signal $CE_{memory\ i}$ with the signal RE or WE from the CPU 2 to produce an area read enable signal $RE_{memory\ i}$ or an area write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area Bi. 9

Regarding Claims 19-21, 28, Koschella discloses CPU2 initiating associated control instructions (e.g., reading or writing) for the memory device 3 during the regular operating cycle, for reading or writing data in an unprotected area of the memory device 3, where the unprotected area does nor require authorization access the authorization logic device 5.1. The JTAG interface (externally accessible Data interface 6) known as Joint Test Action Group (JTAG) is activated via a suitable external signal s1, which in the case of processors and microcontrollers is commonly referred to as "TEST" and "JTAG", respectively. Data d1 can be read or written into the memory device 3 through the externally accessible data interface JTAG 6, or data (D0, .Dn,) can be read or written from the CPU2 during different times.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22- 24 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koschella (US-Patent No. 7,054,121) in view of Golshan (US Patent No. 6,671,841).

Regarding Claims 22- 24, 29-31, Koschella substantially discloses a read enable signal RE or write enable signal WE generated from the CPU 2 and derived from a system CPU clock (not shown), for "reading" or "writing" data in memory device 3, Fig. 8. A JTAG clock is externally provided to the externally accessible data interface JTAG 6, where the two clocks are asynchronous with respect to each other. For a person skilled in the art, it is well known that the JTAG external clock is slower that the system CPU clock. Nevertheless, Koschella does not explicitly disclose a synchronization buffer for synchronizing signals between JTAG, CPU interface and the controller.

In analogous art, Golshan (US Patent No. 6,671,841) discloses a "synchronizer 140" for synchronizing a JTAG clock "TCK 125" to a system clock CPU clock "CLK 135", as shown in the block diagram of a system 10, Fig. 1B and in the flow diagram of a method 400, Fig. 4). It would have been obvious to a person having ordinary skill in

the art at the time the invention was made to incorporate a synchronizer as taught by Golshan, in the processor-memory of Koschella, for eliminating clock skewing associated with asynchronous clocks.

Conclusion

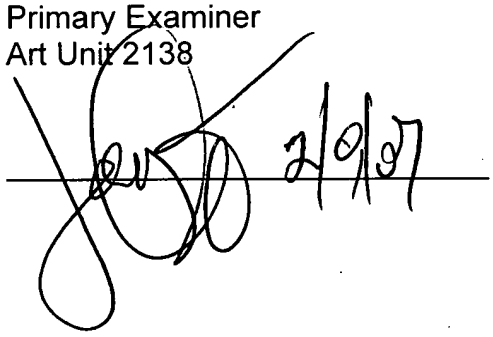
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



Date: 9 February 2007
Office Action: Non-Final Rejection

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